IN THE CLAIMS

Please amend the claims as follows:

Claims 1-143 (Canceled)

144. (New) An integrated circuit comprising:

a monocrystalline Group IV semiconductor substrate;

a compound semiconductor portion including a laser overlying the monocrystalline Group IV semiconductor substrate; and

a Group IV semiconductor portion including an electrical component coupled to the laser, wherein the Group IV semiconductor portion lies within or over the monocrystalline Group IV semiconductor substrate.

145. (New) The integrated circuit of claim 144, further comprising a waveguide, wherein the waveguide is coupled to the laser and to the electrical component.

146. (New) The integrated circuit of claim 144, wherein the electrical component is a transistor.

147. (New) The integrated circuit of claim 144, wherein the Group IV semiconductor portion includes CMOS transistors, of which, the electrical component is one of the CMOS transistors.

148. (New) The integrated circuit of claim 144, further comprising an accommodating buffer layer lying between the monocrystalline Group IV semiconductor substrate and the compound semiconductor portion.

149. (New) The integrated circuit of claim 148, further comprising a waveguide, wherein the waveguide is coupled to the laser and the electrical component, and wherein the waveguide comprises at least a portion of the accommodating buffer layer.

150. (New) The integrated circuit of claim 148, wherein the compound semiconductor portion has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the accommodating buffer layer.

151. (New) The integrated circuit of claim 148, wherein the accommodating buffer layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the monocrystalline Group IV semiconductor substrate.

152. (New) The integrated circuit of claim 148, wherein the integrated circuit has at least one feature selected from a group consisting of:

the accommodating buffer layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the monocrystalline Group IV semiconductor substrate; and

the accommodating buffer layer and the compound semiconductor portion have a lattice mismatch no greater than approximately 2.0% and a thickness of the compound semiconductor portion is at least approximately 20 nm.